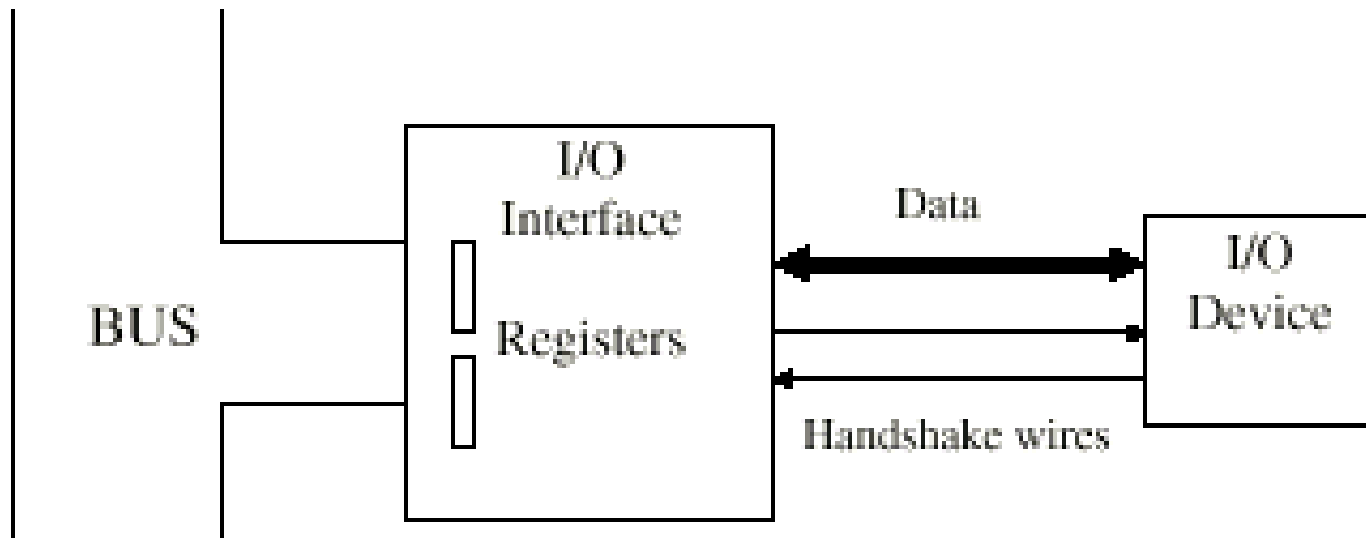


More on Input/Output

- The Computer accesses the I/O device by **reading/writing bit patterns** to one or more registers located in the I/O interface.
- For the computer this is just like reading/writing memory locations. The **I/O Interface** then **interprets** these bit patterns, and carries out the required **action** on the **I/O device**.



Bus Interfacing

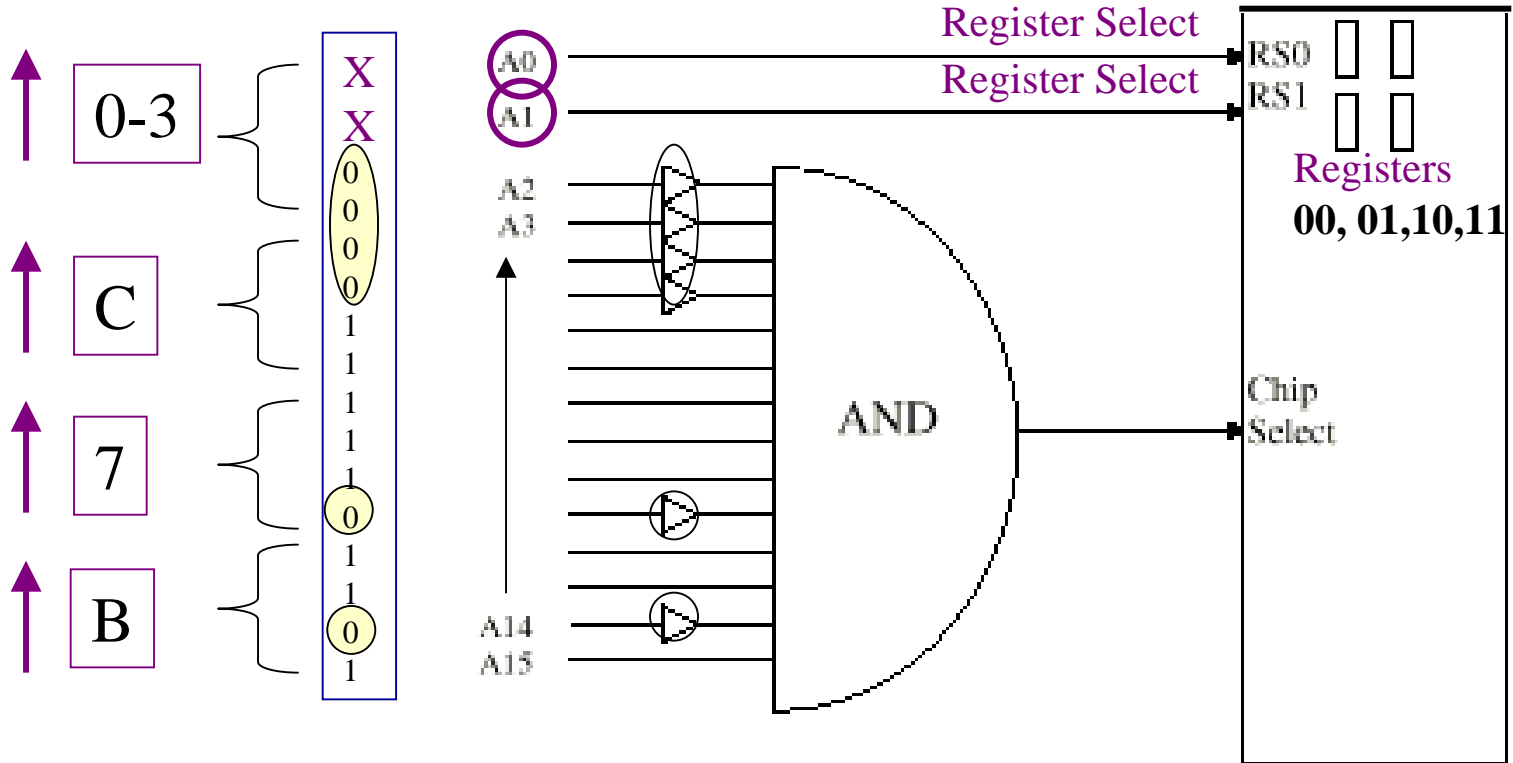
- All I/O devices are controlled and communicated with via a small set of registers.
- Consider a Four Register I/O device, which is to be memory-mapped to memory locations B7C0- B7C3, on a 16-bit computer with an 8-bit data Bus (e.g. Intel 8088)



- For **every address line** for which there is a 0 or a 1 in the above, **create an input to an AND** gate.
- **If 0**, first pass it through an **inverter**, **if a 1** make a **direct connection**.
- The **output of the AND** gate is connected to the I/O Interface **Chip Select** pin.

Bus Interfacing

- Use the two address lines for which there is an **X**, to **select the individual register** on the Interface.



Bus Interfacing

Complete Circuit

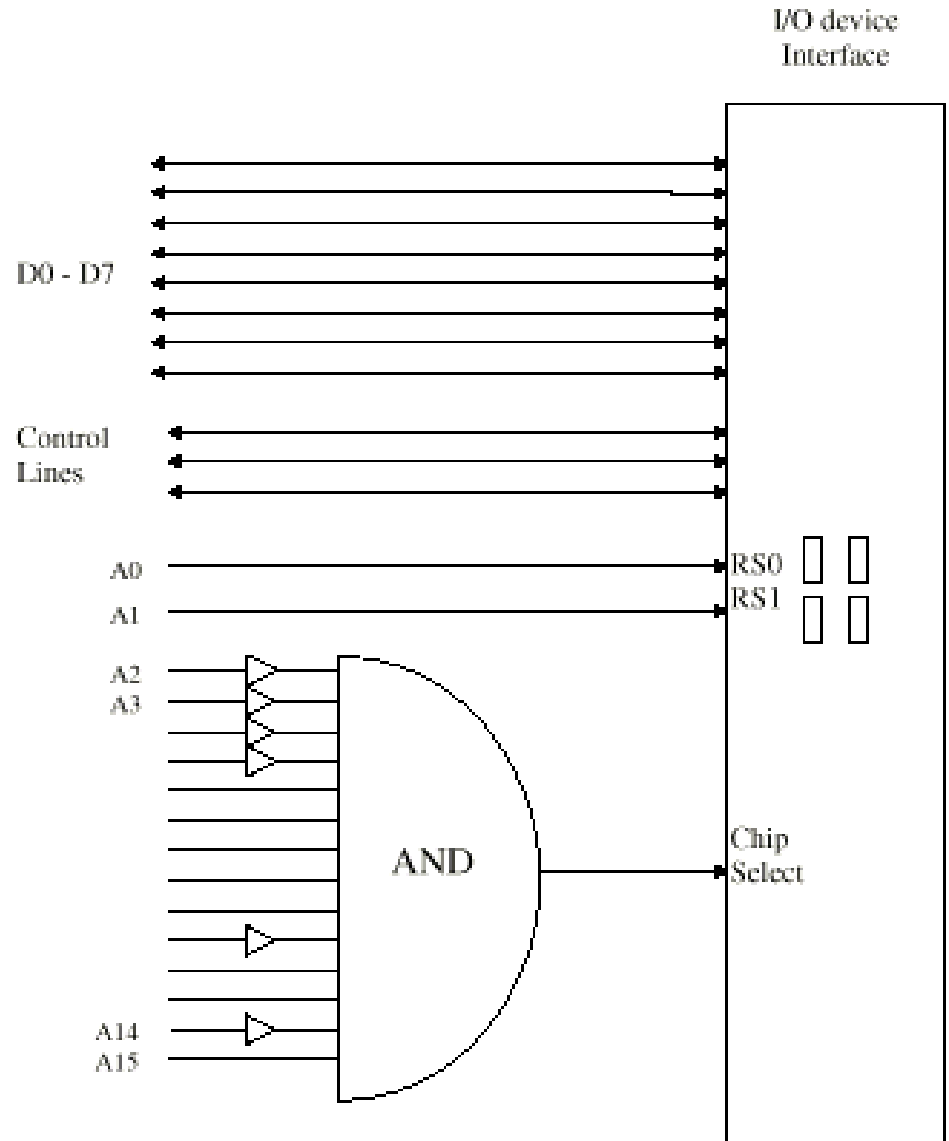
Includes D0-D7 Data Lines.

Control Lines for “handshaking”
with the device

- When the Chip Select pin goes to 1, the I/O interface activates - it knows one of its registers is being addressed.
- A0 and A1 select the individual register (00, 01, 10 or 11)

This Interface is “Fully Decoded”.

Q. What is the effect of disconnecting A15 from the AND gate?
(The interface is now only “partially decoded”).



Bus Interfacing

- Draw the Decode circuitry necessary to map an 8 register I/O device to locations FC00 - FC07.

F C 0 0-7

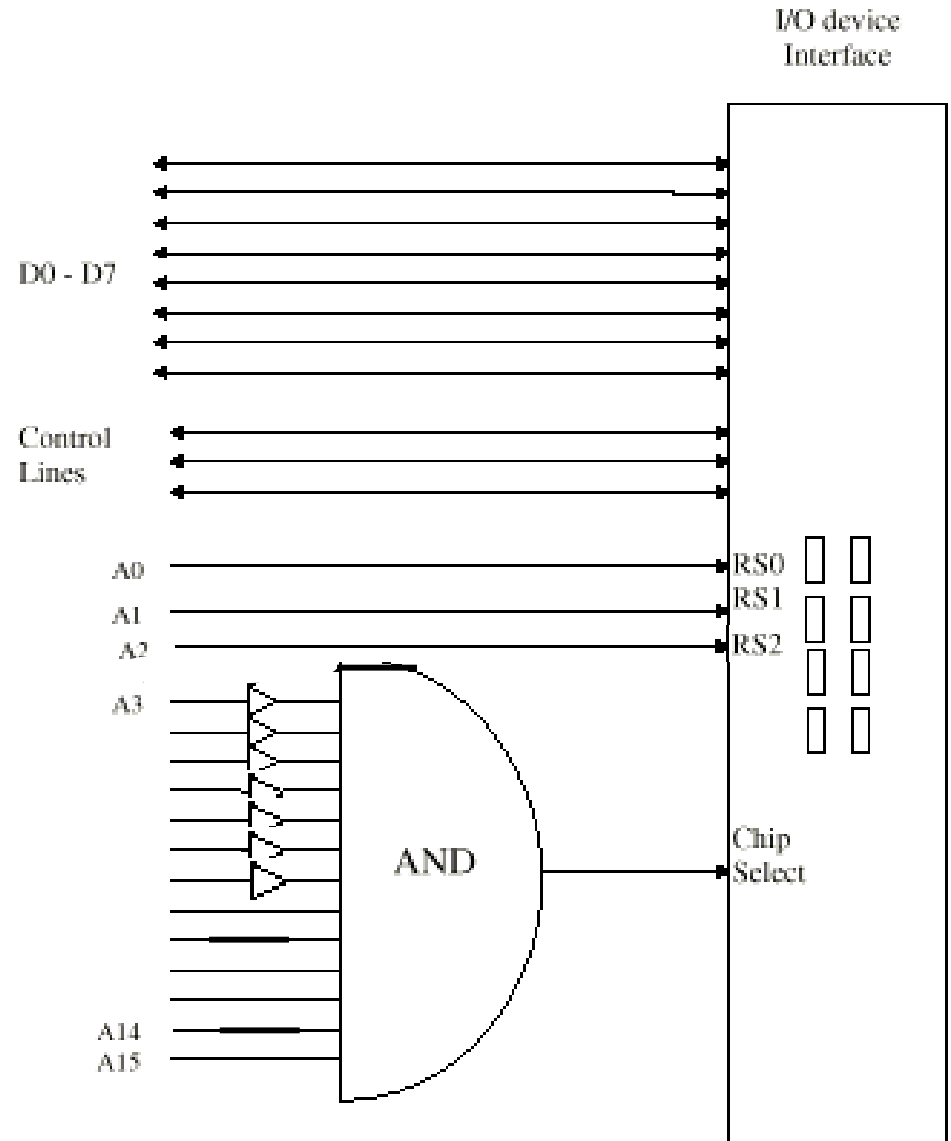
1111 1100 0000 0XXX

0-7

0

C

F



Exercise

- Draw the Decode circuitry necessary to map a 4 register I/O device to locations A310 - A313.
- Draw the Decode circuitry necessary to map an 8 register I/O device to locations CD20 - CD27.
- What is the effect of not including A15 & A14 in the circuit?
- What Addresses now activate the Chip Select?